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Article

Buck-Boost Single-Stage Microinverter for Building Integrated Photovoltaic Systems

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Abstract: Microinverters for Building Integrated Photovoltaic (BIPV) systems must have had a small number of components, be efficient, and be reliable. In this context, a single-phase Buck-Boost Single-stage Microinverter (BBSM) for grid-connected BIPV systems is presented. The concept of topology is extracted from the buck-boost converter. The leakage current in the system is kept under control. It uses an optimal number of active and passive components to function at a high-efficiency level. The suggested topology provides a high level of reliability due to the absence of shoot-through problems. To validate the findings, a simulation in combination with an experimental system for a 70 W system is developed with the design approach. The efficiency of the microinverter, total harmonic distortion of the grid current are measured as 96.4% and 4.09% respectively. Finally, a comparison study has indicated the advantages and disadvantages of the suggested inverter.

Keywords: buck-boost microinverter; building integrated photovoltaic; discontinuous conduction mode



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1. Introduction

The major goal of a Building Integrated Photovoltaic (BIPV) system is to create a net-zero energy buildings with lowering CO₂ emissions in the industry. According to the assessments on BIPV systems market, the global compound annual growth rate is expected to be over 45% from 2010 to 2021 [1,2]. The low-cost thin-film photovoltaic production methods will enhance the BIPV market growth. As a result, BIPV systems have evolved into architectural elements, demanding attributes such as reduced size, ease of grid integration, and the capacity to gather maximum energy in all weather conditions. Inverters that convert DC to AC with high efficiency as well as the low profile is necessary to meet these requirements. For BIPV applications, a microinverter based solution is the best option [3,4]. In this context, some of the advantages of this technique should be mentioned, including:

1. Individual Maximum Power Point Tracking (MPPT) systems capture the most energy;
2. For future development and maintenance, it is scalable with a plug-and-play option;
3. BIPV systems have a high power density while being light in weight;
4. Improved safety because the DC wire can be shortened and the AC cables come down from the roof.

In the market, there are many microinverters for PV modules [5]. However, isolated systems, which are commonly utilised, increase size, weight, and expense. Multiple stage inverters are another frequent arrangement that decreases efficiency and lifespan [6]. Table 1 shows a sample of microinverters that are available at the moment for commercial

use. It demonstrates the maximum capacity, power efficiency, and gross weight of these inverters. It can be shown that at maximum power, the maximum efficiency varies from 94% to 96%. Single-stage transformerless inverters, on the other hand, are built for excellent performance with fewer parts and less energy loss [7].

Table 1. Ratings of microinverters available in market [5].

Microinverter	Maximum Power (W)	η (%)	Weight (kg)
ABB Micro-0.25-I-OUTD	250	96.5	3.5
SMA SB240-US-99	250	95.9	2.9
LS250-AU	250	96.3	2
Darfon MIG300	260	95	2.5
INVOLAR MAC250	250	95	2.9
SBT-250WF	250	94.3	2
SUNCON SC-MAC250A	235	95.2	2.44
RSMI-250L	250	95.5	NA

In [8], various single-stage topologies were investigated. There are several subcategories in this field of research, depending on whether the topologies are formed from boost or buck-boost [8]. The differential boost inverter, which consists of dual boost converters that creates a sinusoidal wave which has 180° phase shift, is described in [9]. The main drawback to this setup is that the high-frequency switches are hard switched, resulting in substantial switching losses and electromagnetic interference. Switching loss issues are addressed in the buck boost half-bridge inverter topology described in [10] by reducing the number of switches operating during each cycle of the reference voltage. Inconvenience with this inverter for BIPV application is that it needs two PV modules on the source side, one of which is used in the half-cycle. The boost microinverter described in [11] was primarily based as a microinverter for roof-top solar Photovoltaic systems, but, the architecture was not suited for BIPV applications due to the usage of bulky inductors. Flying buck-boost inverter that is inductor-based has been described in [12], this has reduced the switching losses through the employment of three power electronics switches for every half a cycle, however the number of components in the conduction path at a given time is higher in this topology, leading to an increased conduction loss. The buck-boost inverter introduced in [13] has minimum switching losses and size with four switches. To boost the voltage, the inverter shown in [14] employs a capacitor-based charge-pump model. It lacks buck-boost capabilities and control of MPPT testing is difficult because of the non symmetric input current, despite being double grounded to avoid leakage current.

Following a thorough analysis of the literature, the design of the single-stage microinverter with the aforementioned features has raised interest:

1. Buck-boosting with reduced losses and heat dissipation by using fewer conduction devices;
2. The influence of EMI and harmonic distortion is reduced when leakage current is kept under the standard limit;
3. Lower power ranges with higher efficiency.;
4. Protection against shoot-through issues.

In this case, this article proposes the Buck-Boost Single-stage Microinverter (BBSM) topology to convert DC power to AC, which satisfies all of the aforementioned requirements. The PV system under consideration uses an appropriate switching approach that allows the inverter to run in Discontinuous Conducting Mode (DCM) and track maximum power using the Perturbation and Observation (P&O) technique [15]. For the first time, this paper describes a number of unique and scientific additions to the BIPV system:

1. With fewer active and passive components, buck-boost capability has been realized.
2. In the lower power range, a better efficiency was achieved.

3. Leakage current value has been reduced within the limit.

The following is an overview of the paper's structure: Principle of operation and analysis of the proposed topology is presented in the next section. Design of passive and active elements of BBSM topology is shown in Section 3. This is followed by a loss analysis in Section 4. In Section 5, design validation of the topology is shown using simulation and experimental results. Finally, conclusions are presented in Section 6.

2. BBSM's Operating Principles and Analysis

The BBSM topology is shown in Figure 1 it encompasses four semiconductor switches controlled devices, two uncontrolled devices (diodes), and a C-type filter. At the Point of Common Coupling, the proposed inverter intersects the grid (PCC). were employed for buck-boost operation and grid injection of PV energy. They also prevent inverter shoot-through issues. This increases system reliability while also making switching processes easier. During both half cycles of the reference, SW_1 and SW_2 are activated to energize the inductors L_P and L_N , respectively. The SW_3 , as well as SW_4 plays a crucial role in inductors' discharge and energy injection into the grid. The load is assumed as pure resistive load R_L .

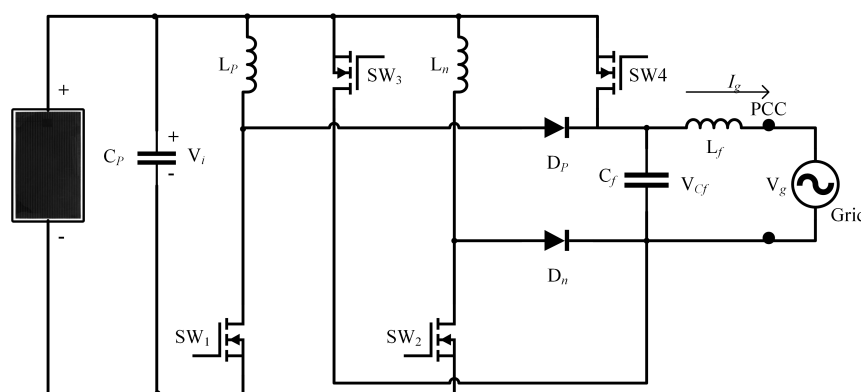


Figure 1. Buck-Boost Single-stage Microinverter.

The SW_1 and SW_2 switches have a high operating frequency. The SW_3 and SW_4 switches operates at low frequency. All of the switches have a built-in safety diode. The inverter can be operated in six distinct modes, three of these modes occurred during each half cycle of the common reference or control signal. These occurred in a row, i.e., one after the other. In both reference cycles, the BBSM topology operates similarly to a typical DC-DC buck-boost converter, except that the suggested inverter topology modulates on a quasi-sinusoidal duty-cycle.

The control strategy is essentially accomplished through a two-steps scheme: the first is achieved via the control of the PV array's voltage by the inductors' current imposition, the second is achieved via the control of the grid current via the output capacitor's voltage imposition. The principle of operations is described with the aid of the control variables are as follows:

1. Parameter O indicates the status of the output voltage half-cycle, during the positive part of the reference, $O == 1$, and switches SW_1 and SW_3 are in the ON state. During the negative part of the reference $O == 0$, and SW_2 and SW_4 are in the ON state. The reference cycle is obtained when V_{ref} is compared to 0.
2. Parameter U indicated when the output voltage V_{Cf} has to be increased $U == 1$, this is achieved through triggering switches SW_3 or SW_4 or to be stepped-down (decreased) then $U == 0$ and achieved when triggering switches SW_1 or SW_2 this is accomplished by comparing V_{ref} and V_{Cf} .
3. Parameter C_P and C_N indicates the charging / discharging process of L_P and L_N , respectively, as follows: $C_P = 1$ & $C_N = 1$, turn on SW_1/SW_2 $C_P = 0$ & $C_N = 1$, turn on $SW_2)/SW_3$ this is generated by comparing the I_{ref} and inductor current I_L .

Table 2 summarises the state of passive and active components in each mode of operation. Figures 2 and 3 depicts the three modes of functioning of the topology in the positive and negative half-cycles, respectively. In different modes, the highlighted components are active. It's vital to remember that during each operation, only one switch is in the conduction path, even if another switch is on. This may help to lower the total power loss of the system.

Table 2. Components operational status at each mode.

Passive Elements			Active Elements			Mode
O	$C_P (C_n)$	U	$SW_1 (SW_2)$	$SW_3 (SW_4)$	$D_P (D_n)$	
1	1 (0)	0	1 (0)	1 (0)	RB (RB)	P_1
1	0 (0)	1	0 (0)	1 (0)	FB (RB)	P_2
1	0 (0)	0	0 (0)	1 (0)	RB (RB)	P_3
0	0 (1)	0	0 (1)	0(1)	RB (RB)	N_1
0	0 (1)	1	0 (0)	0 (1)	RB (FB)	N_2
0	0 (0)	0	0 (0)	0 (1)	RB (RB)	N_3

RB = Reverse bias, FB = Forward bias

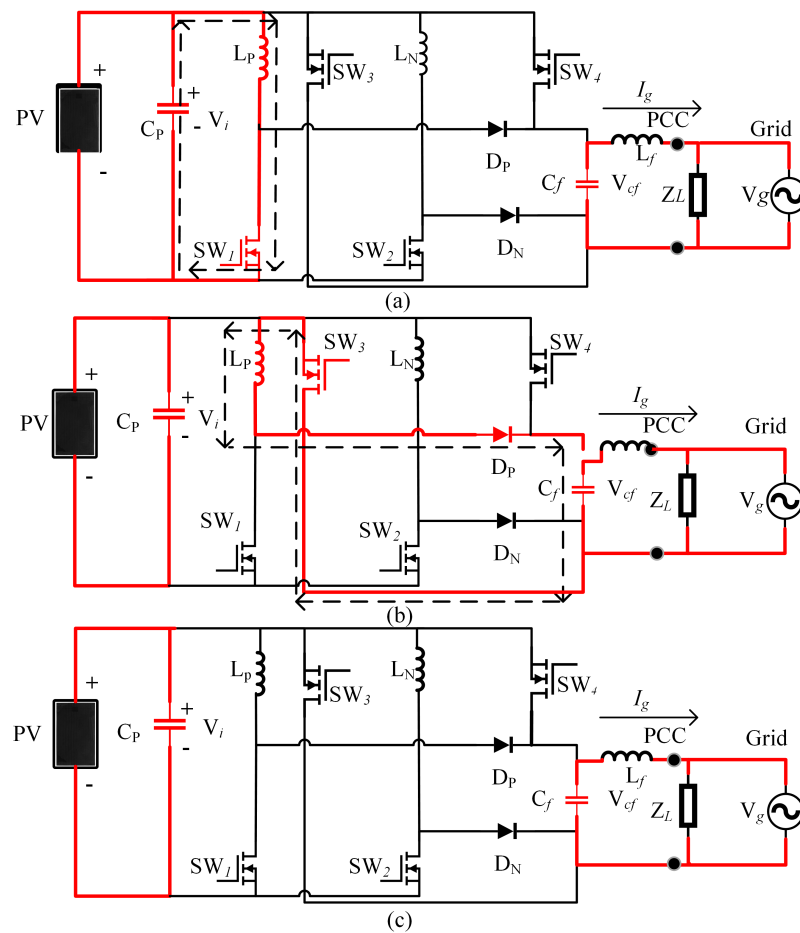


Figure 2. (a) Circuits that are equivalent to Mode P_1 . (b) Circuits that are equivalent to Mode P_1 . (c) Circuits that are equivalent to Mode P_1 .

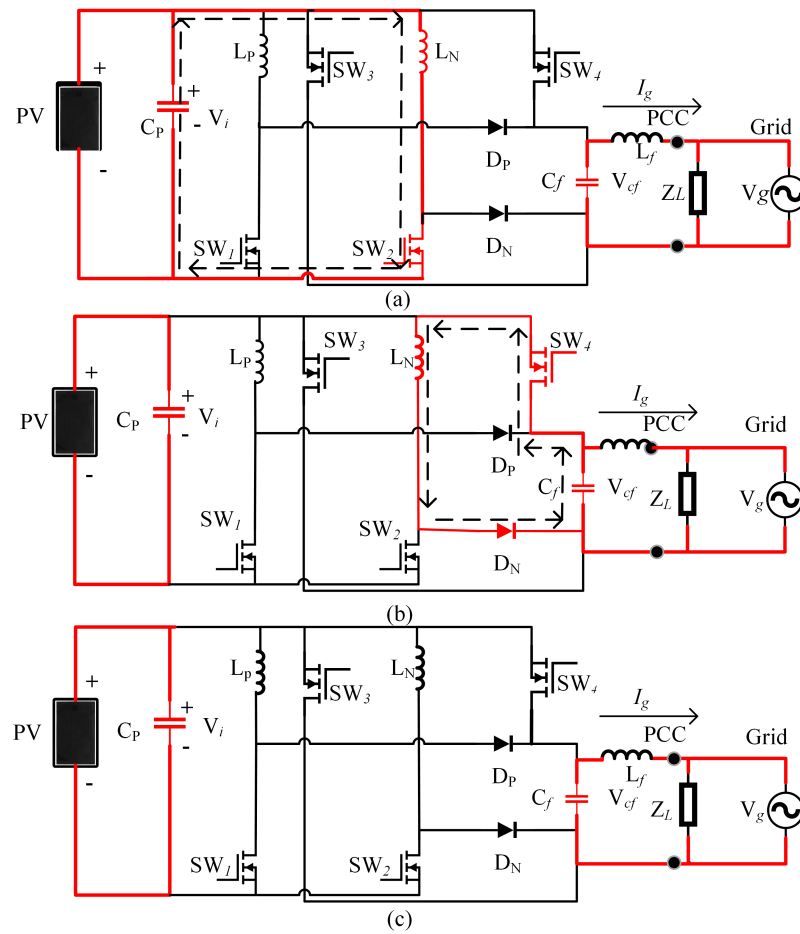


Figure 3. (a) Circuits that are equivalent to Mode N_1 . (b) Circuits that are equivalent to Mode N_2 . (c) Circuits that are equivalent to Mode N_3 .

The operating mode P_1 is carried out for the current assessment of the inductor L_P as shown in Figure 2a, and switch SW_1 is activated due to this reason. Differential equations for control variables are derived from Figure 2a. Here V_i is the input voltage and V_g is the grid voltage, C_f is the output filter capacitor, and R_L is the load.

$$\frac{di_{L_P}(t)}{dt} = \frac{V_i}{L_P} \quad (1)$$

$$\frac{dv_{C_f}(t)}{dt} = \frac{v_g(t)}{C_f R_L} \quad (2)$$

After storing the energy in L_P during P_1 mode to provide the required voltage gain, the P_2 working mode is initiated. The stored energy is transferred through the output filter capacitor–load combination, while the positive half cycle diode D_P becomes forward biased in addition to creating a closed-loop via SW_3 as well as the inductor L_P , meanwhile, SW_1 is turned into its off status. The operating operation can be expressed using the differential equations from Figure 2b as follows;

$$\frac{di_{L_P}(t)}{dt} = -\frac{v_{C_f}(t)}{L_P} \quad (3)$$

$$\frac{dv_{C_f}(t)}{dt} = \frac{i_{L_P}(t)}{C_f} - \frac{v_g(t)}{C_f R_L} \quad (4)$$

When the energy stored in inductor (L_P) is transmitted to capacitor load combination (C_f), the P_3 mode is then initiated. As shown in Figure 2c, the output energy of the filter capacitor is delivered under this mode.

$$\frac{dv_{C_f}(t)}{dt} = -\frac{v_g(t)}{C_f R_L} \quad (5)$$

The N_1 operation mode is employed to apply current to inductor L_N , as shown in Figure 3a, and switch SW_2 is enabled for this reason. The following differential equations for control variables are derived from Figure 3a.

$$\frac{di_{L_N}(t)}{dt} = \frac{V_i}{L_N} \quad (6)$$

$$\frac{dv_{C_f}(t)}{dt} = \frac{v_g(t)}{C_f R_L} \quad (7)$$

After storing sufficient energy in the negative half cycle inductor (L_N) to provide the required voltage gain, the N_2 working mode is activated. The stored energy is delivered to the filter capacitor-load combination, while the diode D_N becomes forward biased in addition, establishes a path of conduction via SW_4 as well as the inductor L_N , SW_2 is triggered off mean. From Figure 3b, the following differential equations are found.

$$\frac{di_{L_N}(t)}{dt} = -\frac{v_{C_f}(t)}{L_N} \quad (8)$$

$$\frac{dv_{C_f}(t)}{dt} = \frac{i_{L_N}(t)}{C_f} - \frac{v_g(t)}{C_f R_L} \quad (9)$$

N_3 mode is activated, when all of the energy from the inductor (L_N) is shifted to the capacitor (C_f). As shown in Figure 3c, the filter capacitor energy can be delivered to the output load in this mode.

$$\frac{dv_{C_f}(t)}{dt} = -\frac{v_g(t)}{C_f R_L} \quad (10)$$

The current flow direction is represented as dashed lines in Figures 2 and 3. To evaluate the proposed topology, the following assumptions are made.

1. Equation (11) shows the relationship between F_g (Grid frequency) and F_{sw} (Switching frequency of switches SW_1 and SW_2).

$$F_{SW} = 2n \times F_g \forall n \in N \quad (11)$$

2. The semiconductor devices device possesses ideal characteristics.
3. Throughout each switching time-period T_{SW} , the grid voltage $v_g(t)$ is considered constant.
4. MOSFETs and diodes have zero forward resistance and infinite reverse resistance.
5. The duty cycle remains constant during each switching period.
6. The inverter's operation is maintained DCM.
7. The load is resistive R_L

The L_P and L_N behave similarly during both reference cycles, they are referred to as L in the analytical section. Inductor current at the peak interval in zoomed in Figure 4b. In P_1 mode, the inductor current increases. For the j th switching period, the inductor charging current I_L achieves its maximum value at $t = t_{ON}(j)$. As the quantity of energy transferred to the output is determined by the magnetizing current of the inductor, the peak value of

the current ($i_{L_{peak}}$) is provided in (12) and depends on the output power. (13) can be used to express the energy stored in the inductor (E_{in}).

$$i_{L_{peak}}(j) = \frac{V_i}{L} D_1(j) T_{SW} \quad (12)$$

$$e_{in}(j) = \frac{1}{2} L i_{L_{peak}}(j)^2 \quad (13)$$

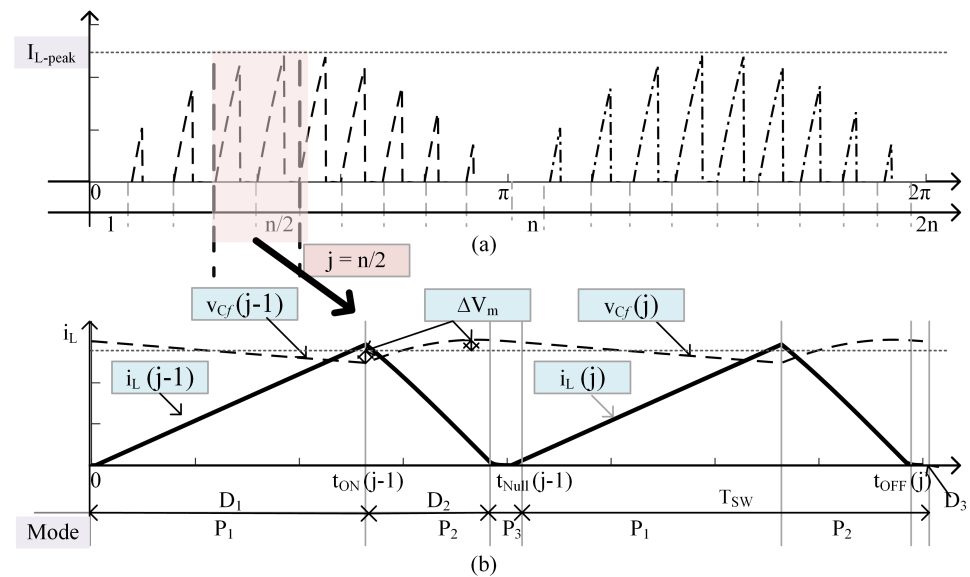


Figure 4. (a) Inductor current (I_L), (b) Inductor current and capacitor voltage during the peak switching interval.

Using Equation (13), the average value of current in inductor I_{avg} throughout a swapping period expressed in Equation (14). As noted in (15), the current at output A is a sinusoidal changing current and that can be expressed as I_g , as illustrated in the expression (14). As a result, the energy required on the output side E_{out} can be written as (16). The peak output voltage is V_m in this case. By equating the Formulas (13) and (16), the charging duty ratio may be stated as (17).

$$i_{avg}(j) = \frac{L i_{L_{peak}}(j)^2}{2 V_i T_{SW}} \quad (14)$$

$$i_g(j) = i_{avg}(j) \sin(\omega t) \quad (15)$$

$$e_{out}(j) = i_{avg}(j) V_m \sin^2\left(\frac{\pi}{n} j\right) T_{SW} \quad (16)$$

$$D_1(j) = \sqrt{\frac{2 L i_{avg}(j) V_m}{V_i^2 T_{SW}}} \sin\left(\frac{\pi}{n} j\right) \quad (17)$$

The discharging duty ratio can be determined as (19).

$$\frac{V_i}{L} D_1(j) T_{SW} - \frac{V_{Cf}}{L} D_2(j) T_{SW} = 0 \quad (18)$$

$$D_2(j) = \sqrt{\frac{2 L i_{avg}(j)}{V_m T_{SW}}} \quad (19)$$

The inverter modulation index is thus indicated by (20) and static gain is given in (21).

$$M = \sqrt{\frac{2LI_{avg}V_m}{V_i^2 T_{SW}}} \quad (20)$$

$$\frac{V_m}{V_i} = \frac{D}{\sqrt{\frac{2L}{R_L T_{SW}}}} \quad (21)$$

2.1. DCM Operational Requirement

The inductor current discharge completely in time $D_2 T_{SW}$, if the average value of the current is lesser than the maximum ripple. Until the next switching cycle, the current will stay zero. When this pattern occurs, the inverter is in DCM mode. If the suggested inverter topology meets DCM condition for the time duration $j = n/2$, it operates in DCM mode throughout the grid cycle. The essential requirement for sampling duration $j = n/2$ of the grid voltage is applied as described in (22) for calculating the peak modulation index M limit for maintaining DCM functioning. In accordance with the conditions, the peak modulation index limit is calculated based on (23).

$$D_1(n/2)T_{SW} + D_2(n/2)T_{SW} = T_{SW} \quad (22)$$

$$M_{max} = \frac{1}{\frac{V_i}{V_m} + 1} \quad (23)$$

The peak output voltage, V_m , is used here.

2.2. Elements for Energy Storage Design

As the physical size of the inverter is determined by the size of its energy storage devices, the design of these elements is critical. Figure 4 depicts the inductor current $i_L(t)$. Energy is delivered in a discrete form since the inverter works in DCM. During each switching interval (T_{SW}) Inductor L will store and transmits energy. Thus, a C_f capacitor is used in the inverter topology. The inductor's energy has been completely transferred to the capacitor C_f . During the peak phase ($j = n/2$), it transfers most of the energy from L to C_f . The inductor should be able to handle ($2P_{max}$), where P_{max} is the maximum input power. This situation assures when the grid receives (P_{max}) during each grid cycle, hence (24) is derived from (13). Equation (25) may be used to calculate the inductor value by replacing (12) into (24). The relationship between L and F_{SW} is seen in Figure 5a from (25). The maximum power output of a Photo-Voltaic module determines the design value of L . This condition ensures that DCM will work at any power level.

$$\frac{1}{2}LI_{L_{Peak}}(n/2)^2 = 2P_{max}T_{SW} \quad (24)$$

$$L = \frac{V_i^2 t_{ON}^2 (n/2)}{4P_{max}T_{SW}} \Rightarrow L \leq \frac{V_i^2 M_{max}^2 T_{SW}}{4P_{max}} \quad (25)$$

The total energy accumulated within the inductor (L) during D_1 is totally released to the capacitor during D_2 , as shown in Figure 4. The variations in the energy over D_2 can be represented in (26). The C_f is designed based on the expression (27). The relationship between F_{SW} and C_f is depicted in Figure 5b from (27)

$$2P_{max}T_{SW} = \frac{C_f[(V_m + \Delta V_m)^2 - (V_m - \Delta V_m)^2]}{2} \quad (26)$$

$$C_f = \frac{P_{max}T_{SW}}{V_m \Delta V_m} \quad (27)$$

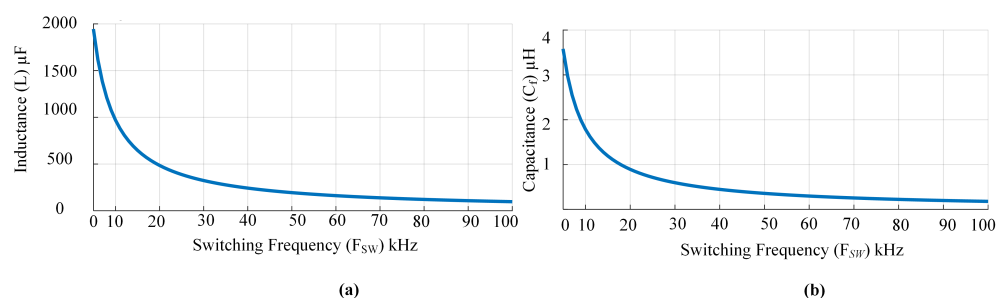


Figure 5. (a) The relationship between the switching frequency (F_{SW}) and the inductance value. (b) The relationship between the switching frequency (F_{SW}) and the capacitance value.

2.3. Power Device Selection

The whole cost and performance of a system are affected by the rating of the power devices in an inverter, which includes storage duration, current gain, and switching frequency. the calculation of voltage, as well as current load on power equipment, can be calculated. Switches maximum voltage is the same as the capacitor's maximum voltage. Similarly, the peak current of the switches matches the maximum inductor current. The total active switch stress SS must be computed if the inverter has k switching devices as stated in (28) using the RMS current I_{RMS_i} and the voltage V_i . Table 3 lists all of the switches RMS current as well as the peak voltage expressions.

$$SS = \sum_{i=1}^k V_i I_{RMS} \quad (28)$$

Table 3. Current and voltage expressions.

Quantity	Relation
$I_{RMS_{SW_1, SW_2}}$	$\frac{V_i T_{SW}}{3L} \sqrt{\frac{M^3}{\pi}}$
$I_{RMS_{SW_3, SW_4}}$	$\frac{T_{SW}}{2L} \sqrt{\frac{V_i^2 M^3}{6V_m}}$
$V_{D_p}, V_{D_n}, V_{SW_3}, V_{SW_4}$	V_m
V_{SW_1}, V_{SW_2}	$V_i + V_m$

3. BBSM Topology Design

The passive elements design relation was derived from the analysis of the BBSM topology, while designing, the nominal power of the inverter is considered equal to the maximum power of the PV module. Thin-film PV modules are widely employed in BIPV applications, according to [16]. For the purpose of inverter validation, we have looked at the first solar PV module. $V_g = 110$ V, $P_{max} = 70$ W, $F_g = 50$ Hz, $V_i = 73$ V. On the basis of Figure 5, the optimal switching frequency of 50 kHz was chosen, resulting in $2n = 1000$. For these specifications, the maximum modulation index is derived using (23) as $M_{max} = 0.68$. The peak permissible inductance for the discontinuous mode of operation (DCM) is estimated using (25) as $L \leq 177$ μH. Black dotted line in Figure 6a shows the two constraints $L \leq 177$ μH and $M_{max} = 0.68$ for the determination of the inductance value. It can be shown that these two constraints are satisfied when the inductance value is 160 μH. The filter capacitor value C_f for output voltage is plotted in Figure 6b based on (27). The capacitance value is between 0.4 μF and 0.5 μF for a peak ripple of 10%. Thus, in this project 0.47 μF capacitor is chosen. The DC-link capacitor C_p is determined as 220 μF for this project [13].

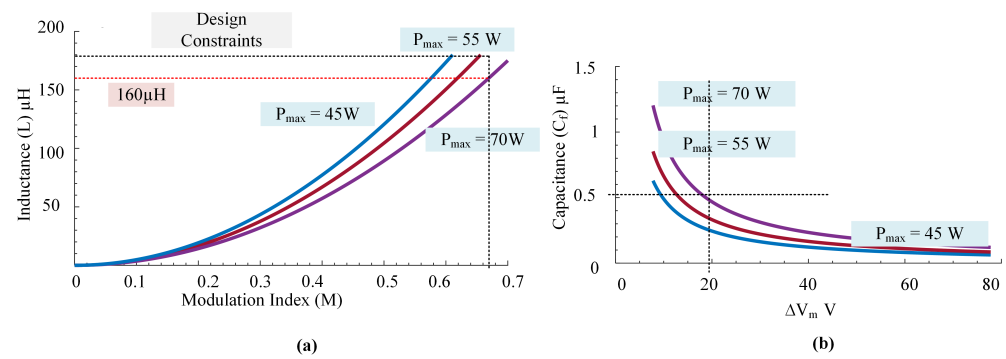


Figure 6. (a) Inductance value vs. modulation index. (b) ΔV_m versus capacitance value for various power ratings.

4. Loss Analysis

Using the elements design value the expected losses of the BBSM topology is discussed in this section. The power loss analysis includes core loss, conduction loss and switching loss evaluation.

4.1. Core Loss

Changing magnetic flux fields causes core loss within a material. The core loss density (P_L) is a function of ΔB , and f_{SW} , where (ΔB) is half of the flux swing as shown in (29). In order to approximate the constants core loss charts are utilised.

$$P_L = a \frac{\Delta B^b}{2} f_{SW}^c \quad (29)$$

Here flux swing ΔB is given in (30).

$$\Delta B = \frac{N \Delta I_{L_{avg}} \mu_0}{l_g} \quad (30)$$

$$\Delta I_{L_{avg}} = \frac{I_{L_{peak}} \sum_{k=1}^n \sin\left(\frac{\pi}{n} k\right)}{n} \quad (31)$$

Number of turns (N). The ripple current in the inductor is ΔI_L , and the air gap in the magnetic core is l_g . The permeability of the air gap is μ_0 , which is $4\pi \times 10^{-7}$. As a result, the equation for P_{core} is (32)

$$P_{core} = P_L l_e A_e \quad (32)$$

The magnetic core's mean path length is l_e , and the cross-sectional area is A_e .

4.2. Conduction Loss

The total conduction loss is equal to the summation of the inductor loss and conduction loss in power devices.

The inductor conduction loss P_{cond_L} can be calculated using the average inductor current as well as the inductor's series resistance R_L from the (33).

$$P_{cond_L} = I_{L_{avg}}^2 R_L \quad (33)$$

In the BBSM, the switch SW_3 , as well as switch SW_4 , operates in a symmetrical way for both half cycles, resulting in the same conduction losses, as determined by (34).

$$P_{cond_{SW_{3,4}}} = I_{RMS_{SW_{3,4}}}^2 R_{ds} \quad (34)$$

The conductive loss of a diode is estimated as (36) using the power loss accompanied with the fixed voltage drop (V_{FV}) as well as the resistance R_{ak} .

$$P_{cond_{D_{P,N}}} = I_{RMS_{D_{P,N}}}^2 R_{ak} + I_{RMS_{D_{P,N}}} V_{FV} \quad (35)$$

Here, the $I_{RMS_{D_{P,N}}}$ is given in Table 3, R_{ak} and V_{FV} are determined from the datasheet of the diode.

4.3. Switching Loss

The switching loss of SW_3 and SW_4 switches is negligible since they operate at a low switching frequency. Similarly, because the inverter works in DCM, the diode's switching loss owing to reverse recovery is zero. Due to the DCM operation, turn on losses are nil in switches SW_1 and SW_2 . As a result, the inverter's total switching losses are indicated in (36).

$$P_{SW_{1,2}} = \frac{<V_{sw}>_T <I_{sw}>_T}{2} f_{sw} t_f + E_{OFF} f_{sw} \quad (36)$$

The switch's Turn OFF energy loss E_{OFF} as well as fall time t_f may be found in the datasheet. The inverter's losses are estimated using the parameters reported in Table 4. The BBSM inverter's power loss is documented in Table 5. All topologies losses are computed using a 70 W system.

Table 4. Power loss calculating parameters.

Number of turns N	74
Air gap in the magnetic core l_g	2 mm
Inductor resistance R_L	6.75 m Ω
Permeability of air gap μ_o	$4\pi \times 10^{-7}$
ON state resistance of Diode R_{ak}	0.03 Ω
Mean path length of magnetic core l_e	171.1 mm
Turn OFF energy loss E_{OFF}	0.015 mWs
Falling time t_f	4.5 ns
Cross sectional area A_e	49 mm ²
Fixed voltage drop V_{FV}	1.5 V
ON state resistance of MOSFET R_{ds}	0.43 Ω

Table 5. The Power loss of the BBSM inverter.

Losses	
SW Conduction losses	2.44
SW Switching losses	5.18×10^{-3}
D Conduction losses	0.72
Inductor core loss	0.89
Inductor copper loss	0.52

5. Design Validation

In order to validate the proposed BBSM topology a simulation and experimental test has been conducted as given below.

5.1. Simulation Results

The simulation using MATLAB / Simulink is carried out for the proposed microinverter and the ratings, as well as component values are displayed in Table 6. A thin film Photovoltaics module FS 270 which is of 70 W is considered, with the approaches given in [17,18] are being used to simulate it for simulation. Figure 7a,b show the I-V and P-V graphs generated from the model for 1 kW/m², 0.8 kW/m² and 0.6 kW/m², respectively.

The testing control circuit and the block diagram of the inverter is given in (20) and plotted in Figure 8, respectively. In this project, the Perturbation and Observation ($P\&O$) approach suggested in [19] is employed for MPPT by sampling I_{PV} and V_{PV} . At a maximum power of 70 W, Figure 9a,b show the current flow through the inductors L_P and L_N , respectively. The theoretical calculations of the peak current through the inductor $I_{L_{Peak}}$ and M_{max} for the DCM functioning of the BBSM inverter topology is convincingly validated. At the maximum power rating, the inverter's output voltage and current are 110 V and 0.636 A, respectively, as shown in Figure 10a. The active power P and reactive power Q in the grid are plotted in Figure 10b.

Table 6. Element values obtained from the design [5].

Input Parameters	$I_{max} = 0.96 \text{ A}$, $V_{max} = 73 \text{ V}$
Output Parameters	$I_{RMS} = 0.63 \text{ A}$, $V_{RMS} = 110 \text{ V}$, $P_{max} = 70 \text{ W}$
Switching Devices	Diode—FEP30JP-4 MOSFET—FQP10N20C Gate driver—TLP350
Capacitor	$C_P = 220 \mu\text{F}$, $C_f = 0.47 \mu\text{F}$, MPX2250V _{AC} , Film capacitor
Inductor (L_P , L_N)	$R_{DC} = 14 \text{ m}\Omega$, $160 \mu\text{H}$, $I_{L_{Peak}} = 6.2 \text{ A}$

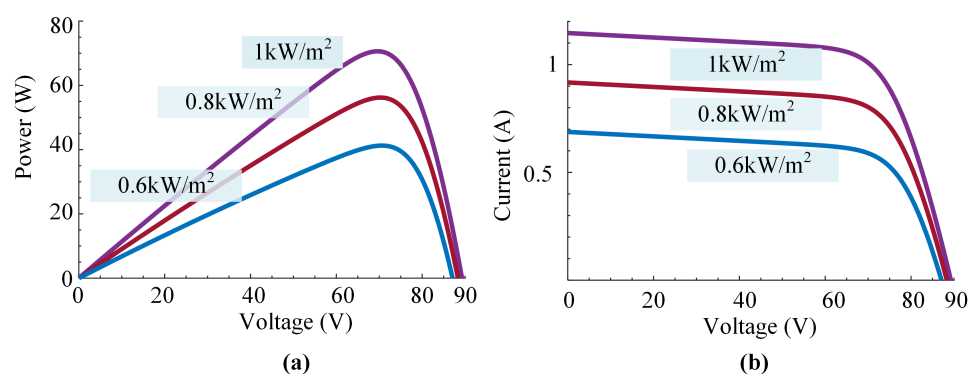


Figure 7. (a) PV voltage index versus Power. (b) PV voltage versus current for different irradiation level.

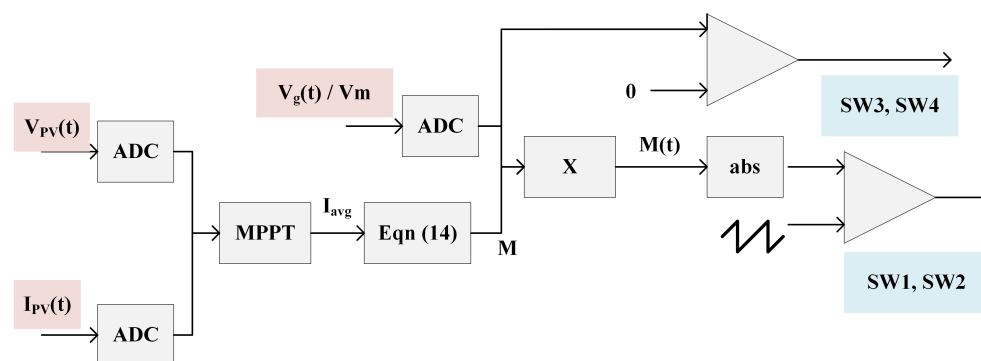


Figure 8. Block diagram of the control technique used for BBSM.

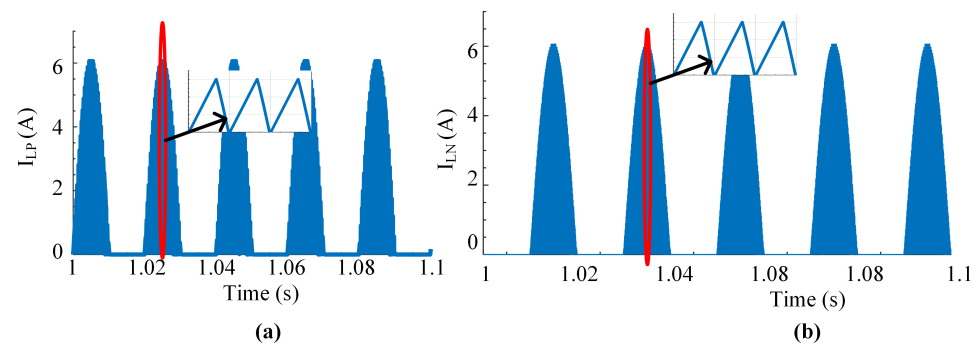


Figure 9. (a) Current through inductor L_P . (b) Current through inductor L_N .

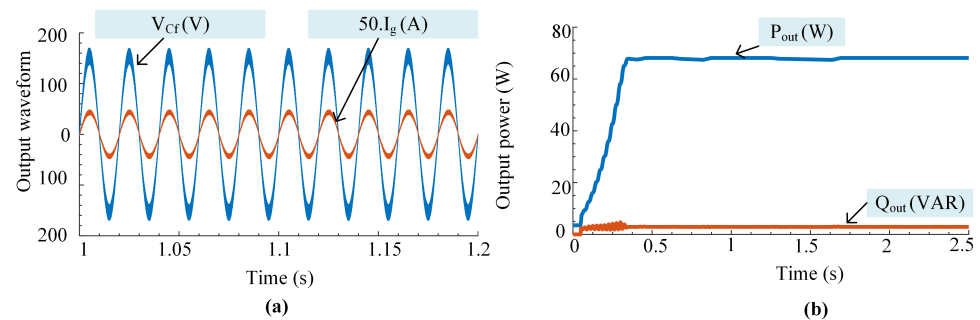


Figure 10. (a) Injected current and output voltage. (b) Active and reactive power at the output side.

Further research of the suggested inverter's open-loop control was conducted by changing the degree of irradiation level. The MPPT operation is shown in Figure 11a while adjusting the level of irradiation (0.8 kW/m^2 to 1 kW/m^2) in 1.25 s. Despite the fact that it functions in the MPP field, further research in this area is essential for exact operation. During irradiation change, Figures 11b and 12a,b show alterations in output current, output power, and input voltage, respectively. The results show that the inverter is operating correctly when the irradiation changes.

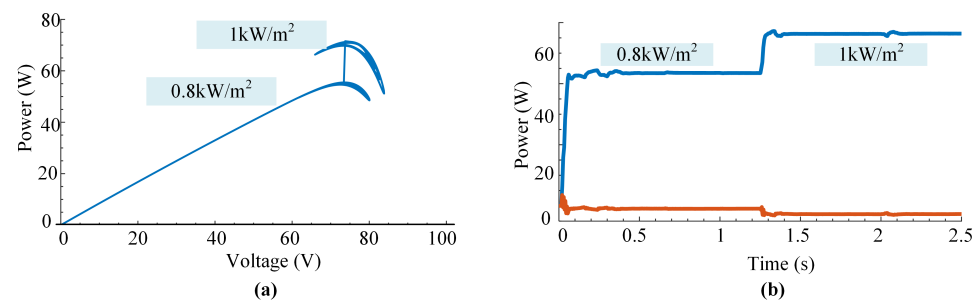


Figure 11. (a) $P - V$ curve of MPPT. (b) Changes in active and reactive power under irradiation.

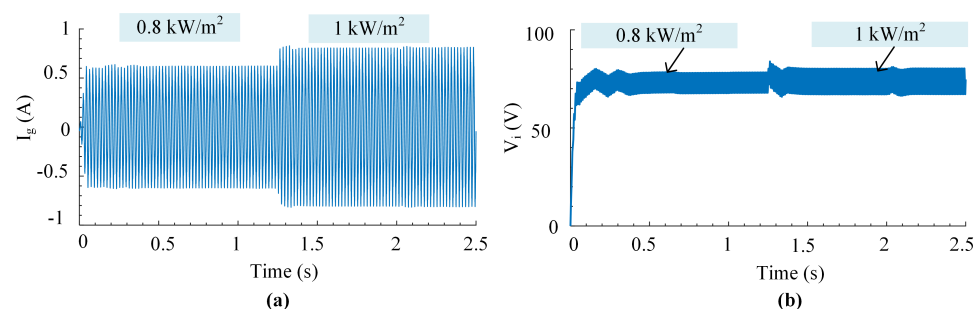


Figure 12. (a) Variation in the output current I_g . (b) Variation in input voltage V_i with respect to changes in irradiation levels.

To evaluate the flow of leakage current in the proposed inverter, a parasitic capacitance of 70 nF was used in the simulation [20]. According to German regulations DIN VDE 0126-1-1, if the leakage current exceeds 300 mA (RMS), the inverter must be removed from the grid. As shown in Figure 13, a circuit for resonance condition is created for the transformerless inverter. PV parasitic capacitance (C_{PV}) as well as filter inductor (L_f) are included in the resonant circuit. X and Y are the inverter's terminals, which are coupled to the single-phase grid via L_f . As shown in Figure 13, the inverter may be simplified into an equivalent circuit consisting of V_{XN} and V_{YN} . As a result, leakage current is determined by V_{XN} as well as V_{YN} . (37) can be used to define the Common Mode Voltage (CMV). The leakage current travels via the parasite capacitance and to the grid when there is a V_{CM} differential. As demonstrated in Figure 14, the proposed topology has low-frequency components V_{XN} and V_{YN} . As the voltage differential between the BIPV module's ground and the grid is low-frequency, the parasitic capacitance's equivalent impedance is high. This high impedance, as seen in Figure 15, restricts the flow of leakage current $I_{Leakage}$. In this simulation, a parasitic capacitance of 70 nF was employed to check the $I_{Leakage}$ [20]. The proposed inverter's leakage current is negligibly tiny, as shown in Figure 15.

$$V_{CM} = \frac{V_{XN} + V_{YN}}{2} \quad (37)$$

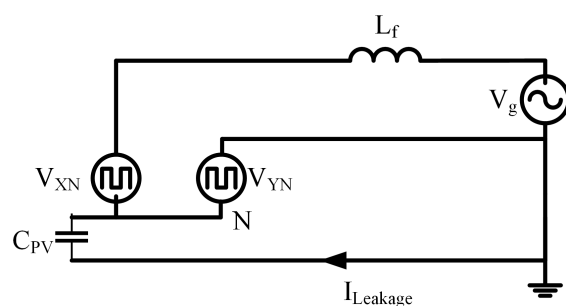


Figure 13. BBSM equivalent circuit to show path for leakage current.

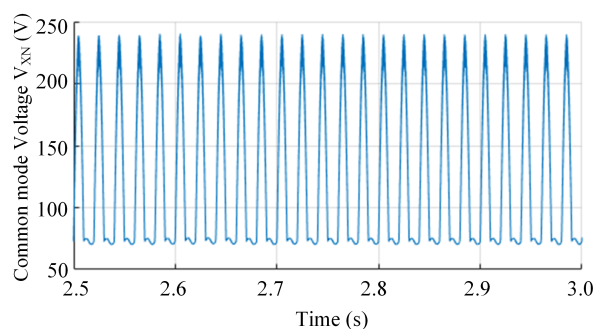


Figure 14. Common mode voltage V_{XN} .

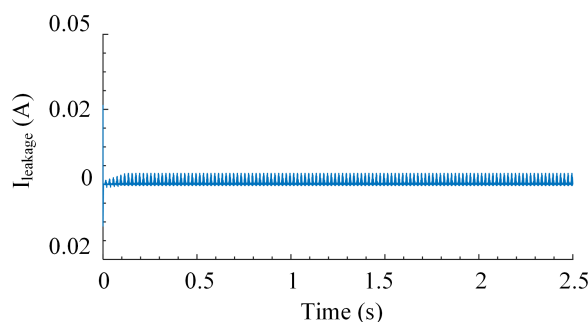


Figure 15. Leakage current at $P_{max} = 70$ W.

5.2. Experimental Results

Based on the specifications in Table 6, an experimental model of a 70 W, 110 V, 50 Hz inverter was designed. In Figure 16a, the experimental settings in the laboratory are shown, and in Figure 16b, the proposed BBSM topology is shown. In the experimental research, the chroma programmable DC power supply 62150H-600S solar array simulator was utilized to simulate the identical simulated Photovoltaic module characteristics. For loading, the programmable AC/DC electronic load 63802 was employed. A chroma 3-phase programmable AC source 61704 was used to duplicate the grid. The switching strategy was created in MATLAB in addition it is linked to the dSPACE-1104 control desk in the control area. All waveforms were captured using a DSOX3014 oscilloscope.

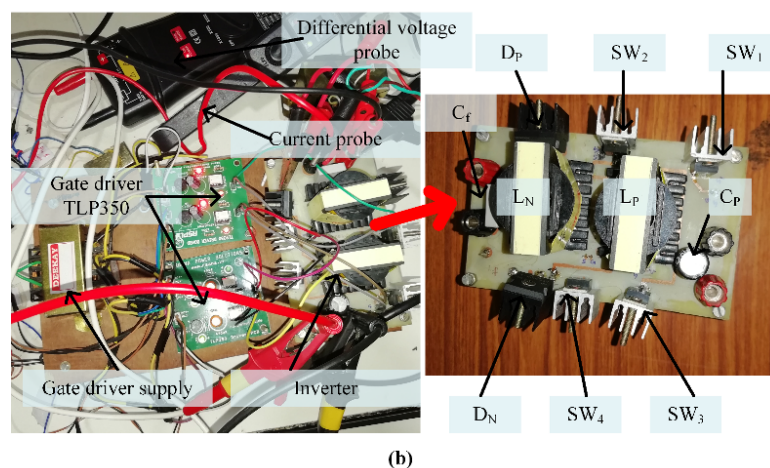
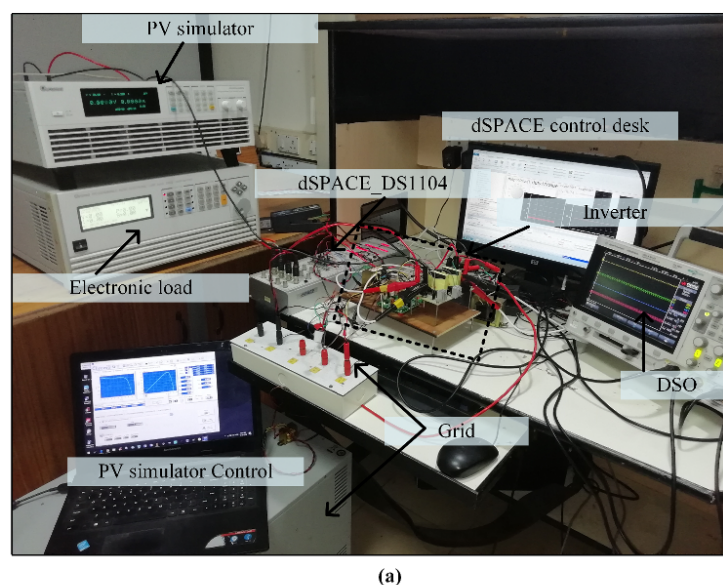


Figure 16. (a) Setup for the experiment. (b) Power circuit of BBSM.

Figure 17 shows the switching pulses created by the dSPACE-1104 by using the TLP350 gate driver. As mentioned in the theory, SW_1 as well as SW_2 , represent 50 kHz pulses, while SW_3 and SW_4 represent pulses at 50 Hz. Currents through L_P and L_N with a magnified view during $P_{max} = 70$ W are shown in Figure 18. It clearly validates the inverter's DCM functioning and $I_{L_{Peak}}$ of around 6 A during $P_{max} = 70$ W, as described in the theoretical analysis. Figure 19 shows the output voltage and current in relation to the input voltage and current at steady state. The output voltage and current RMS values are the same

around the values analyzed and simulated. From Figure 19 the efficiency is obtained is 96.4% as given in (38). As expected from the theoretical analysis efficiency is above 95%.

$$Efficiency(\%) = \frac{(109.84 \times 0.6116)}{71.8 \times 0.97} \times 100 = 96.4 \quad (38)$$

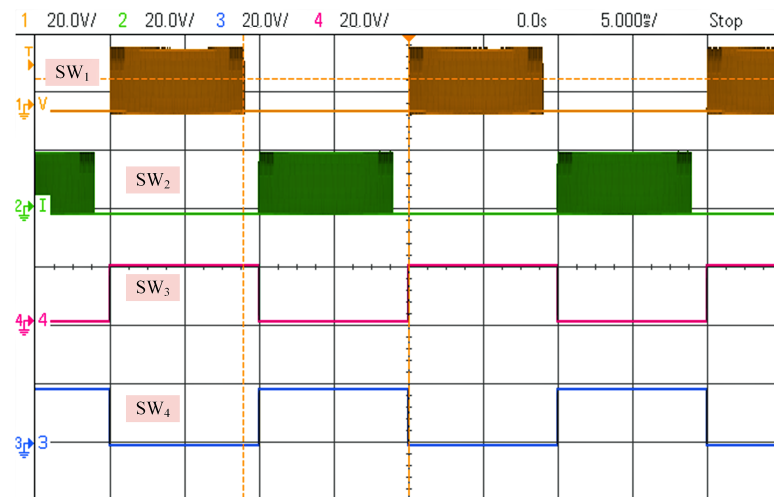


Figure 17. Switching pulses at $P_{max} = 70$ W.

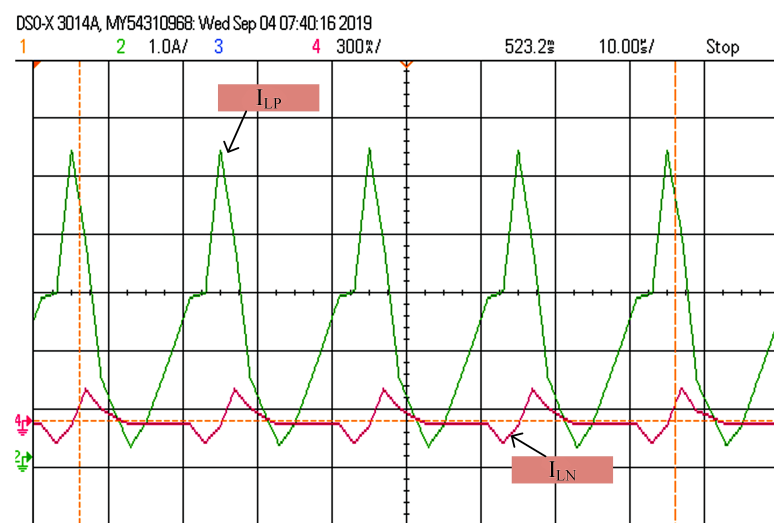


Figure 18. Inductor currents I_{LP} and I_{LN} during $P_{max} = 70$ W.

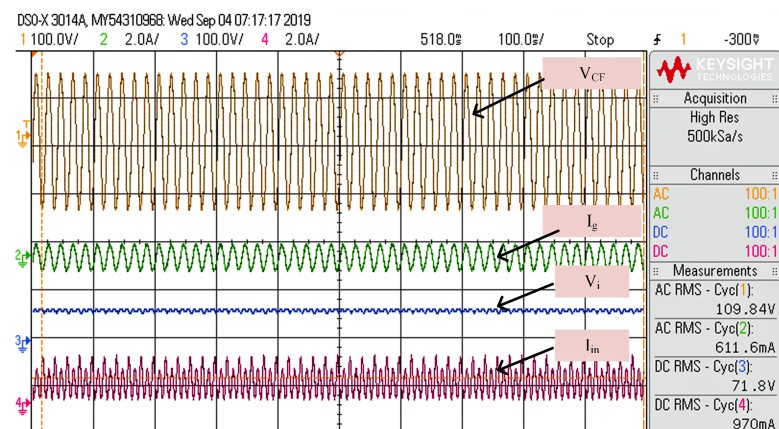


Figure 19. Steady-state output and input voltage and current waveforms during $P_{max} = 70$ W.

The waveforms of real power, phase angle, reactive power, current, voltage, power factor, and apparent power during $P_{max} = 70$ W are shown in Figure 20. It is evident that the power factor is approximately 1. The injected current from the inverter's Total Harmonic Distortion (THD) and Fast Fourier Transform (FFT) values are shown in Figure 21. The THD value of the current fed to the grid is around 5%. The input current, voltage, and steady-state output at 0.8 kW/m^2 are shown in Figure 22, along with the efficiency calculation. Various input voltages inverter efficiency curve is shown in Figure 23. Voltage across and current through the MOSFETs and Diodes are shown in Figures 24 and 25 respectively. The various values of efficiency from the proposed topology in low to nominal power operation is determined using a DC power supply in addition to a resistive load. Table 7 tabulates the comparison between simulation and experimental results, it clearly shows that due to the use of real time elements efficiency during experimental test is slightly lower.

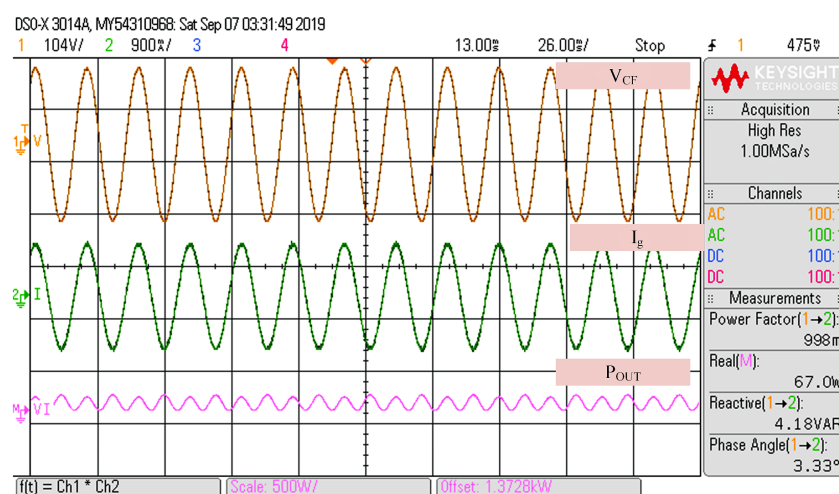


Figure 20. Power quality measurements during $P_{max} = 70$ W.

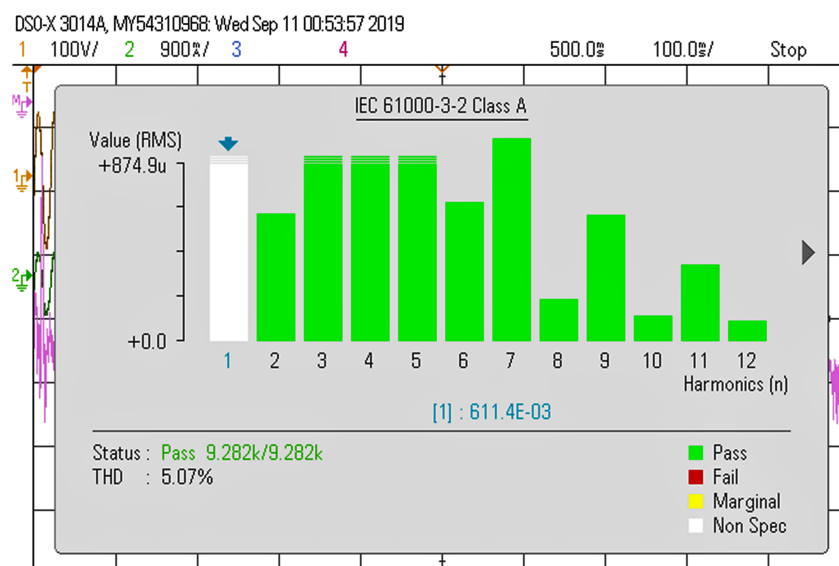


Figure 21. THD of injected current at $P_{max} = 70$ W.

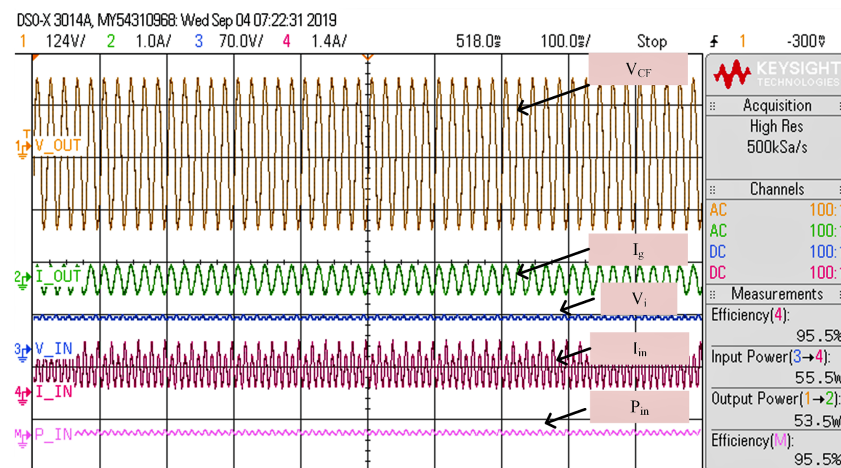


Figure 22. Input and output voltage and current with efficiency at 800 W/m².

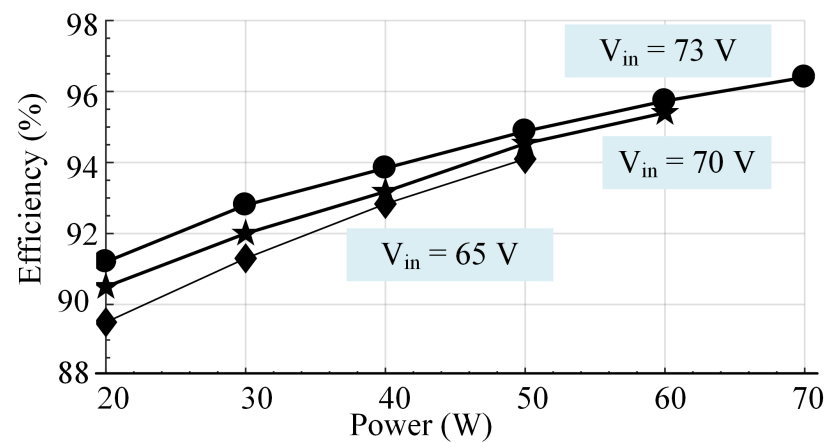


Figure 23. Efficiency curve of the proposed inverter.

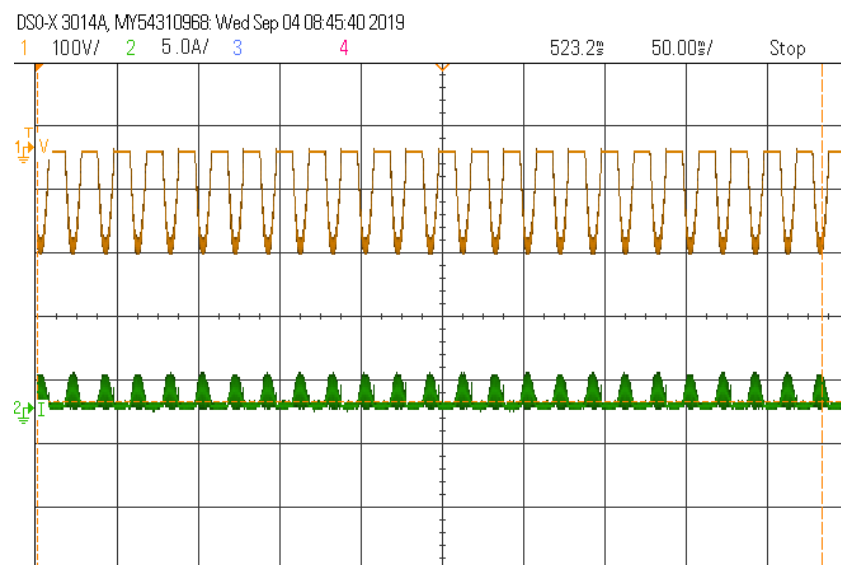


Figure 24. Voltage across and current through the MOSFET.

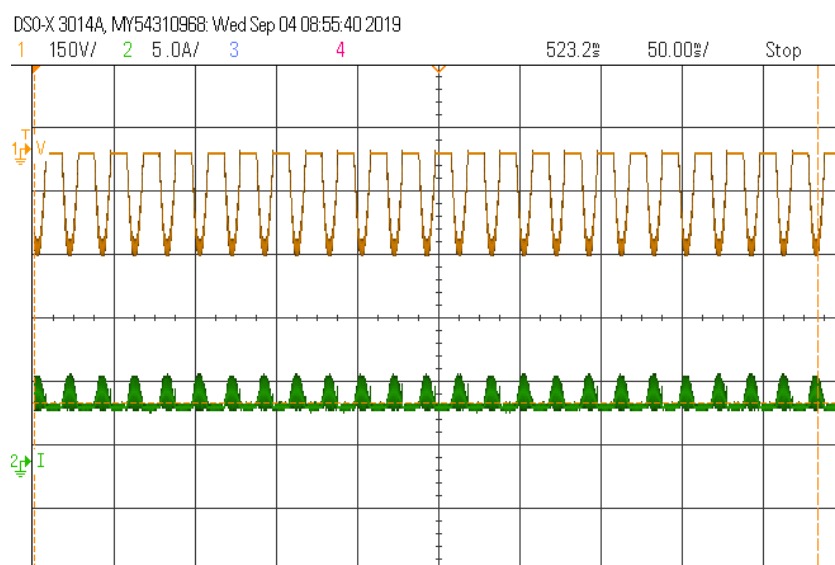


Figure 25. Voltage across and current through the Diode.

Table 7. Comparison of results obtained using simulation and experimental study.

	Simulation Results	Experimental Results
$I_{L_{Peak}}$	6 A	5.6 A
Efficiency	98	96.4
Output voltage ($V_{g_{RMS}}$)	110 V	109.84 V
Output Current ($I_{g_{RMS}}$)	0.624 A	0.614 A
THD	2.83%	4.09%

5.3. Comparison of Topologies

The BBSM uses fewer switches in the conduction path, according to a comparison of other microinverters in Table 8. Other topologies efficiency were determined using the same criteria used in this study. The BBSM topology is more efficient and has less passive elements than other topologies, making it excellent for BIPV applications. Furthermore, the proposed inverter has a negligible leakage current. When compared to other microinverters, BBSM is more efficient and reliable due to the employment of an appropriate number of components in the conduction channel.

Table 8. Comparison of different topologies [5].

	[14] 2017	[21] 2017	[22] 2017	[20] 2017	[12] 2018	[23] 2018	[24] 2019	BBSM
Number of switches	4	4	5	4	5	6	7	4
Number of switches in conduction	2	2	3	2	2	3	4	1
Number of capacitor	3	2	2	1	1	2	3	1
voltage stress of switches	$> V_m$	$> V_m$	$> V_m$	$> V_m$	$> V_m$	$> V_m$	$> V_m$	$> V_m$
Number of diode	6	2	0	4	0	2	3	2
Number of inductor	2	3	2	3	2	2	4	2
Shoot through problem	Yes	No	No	No	No	No	Yes	No

Table 8. Cont.

	[14] 2017	[21] 2017	[22] 2017	[20] 2017	[12] 2018	[23] 2018	[24] 2019	BBSM
Leakage current (mA)	≈22.7	≈0	≈0	≈22.9	≈0	≈0	NA	≈0
Efficiency (%)	93.4	93.6	94.2	92.4	90.27	89	93.8	96.4

6. Conclusions

A buck-boost single-stage microinverter (BBSM) with fewer number of elements, with high efficiency and reliability were proposed in this paper. Due to the limited number of components, a higher performance is achieved. Design details of all the elements were derived in the paper. MATLAB/Simulink simulation and experimental setup was used to verify the design technique of the inverter systems. The results of the BBSM topology shows that it had negligently low leakage current with buck-boost performance, high operational efficiency, THD level for the injected current is within the limit, and prevented shoot-through. According to a comparison examination of the proposed inverter with similar topologies it shows that proposed topology can be recommended topology for Building Integrated PV system.

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References

- Li, G.; Xuan, Q.; Akram, M.; Akhlaghi, Y.G.; Liu, H.; Shittu, S. Building integrated solar concentrating systems: A review. *Appl. Energy* **2020**, *260*, 114288. [\[CrossRef\]](#)
- Mousa, O.B.; Kara, S.; Taylor, R.A. Comparative energy and greenhouse gas assessment of industrial rooftop-integrated PV and solar thermal collectors. *Appl. Energy* **2019**, *241*, 113–123. [\[CrossRef\]](#)
- Bastidas-Rodriguez, J.D.; Franco, E.; Petrone, G.; Ramos-Paja, C.A.; Spagnuolo, G. Maximum power point tracking architectures for photovoltaic systems in mismatching conditions: A review. *IET Power Electron.* **2014**, *7*, 1396–1413. [\[CrossRef\]](#)
- Zare, M.H.; Mohamadian, M.; Beiranvand, R. Single-stage AC module with series power decoupling capability for connecting PV to a single-phase power grid. *IET Power Electron.* **2016**, *10*, 517–524. [\[CrossRef\]](#)
- Chander, A.H.; Kumar, L. MIC for reliable and efficient harvesting of solar energy. *IET Power Electron.* **2018**, *12*, 267–275. [\[CrossRef\]](#)
- Ahmad, A.A.; Abrishamifar, A.; Samadi, S. Low-frequency current ripple reduction in front-end boost converter with single-phase inverter load. *IET Power Electron.* **2012**, *5*, 1676–1683. [\[CrossRef\]](#)
- Hu, Y.; Du, Y.; Xiao, W.; Finney, S.; Cao, W. DC-link voltage control strategy for reducing capacitance and total harmonic distortion in single-phase grid-connected photovoltaic inverters. *IET Power Electron.* **2015**, *8*, 1386–1393. [\[CrossRef\]](#)
- Mathew, D.; Naidu, R.C. Investigation of single-stage transformerless buck-boost microinverters. *IET Power Electron.* **2020**, *13*, 1487–1499. [\[CrossRef\]](#)
- Jha, K.; Mishra, S.; Joshi, A. High-quality sine wave generation using a differential boost inverter at higher operating frequency. *IEEE Trans. Ind. Appl.* **2014**, *51*, 373–384. [\[CrossRef\]](#)
- Wang, C.M.; Chen, T.J. Novel single-stage half-bridge series-resonant buck-boost inverter. *IEEE Trans. Aerosp. Electron. Syst.* **2004**, *40*, 1262–1270. [\[CrossRef\]](#)
- Gao, M.; Chen, M.; Zhang, C.; Qian, Z. Analysis and implementation of an improved flyback inverter for photovoltaic AC module applications. *IEEE Trans. Power Electron.* **2013**, *29*, 3428–3444. [\[CrossRef\]](#)

12. Azary, M.T.; Sabahi, M.; Babaei, E.; Meinagh, F.A.A. Modified single-phase single-stage grid-tied flying inductor inverter with MPPT and suppressed leakage current. *IEEE Trans. Ind. Electron.* **2017**, *65*, 221–231. [[CrossRef](#)]
13. Jain, S.; Agarwal, V. A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking. *IEEE Trans. Power Electron.* **2007**, *22*, 1928–1940. [[CrossRef](#)]
14. Ardashir, J.F.; Sabahi, M.; Hosseini, S.H.; Blaabjerg, F.; Babaei, E.; Gharehpetian, G.B. A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications. *IEEE Trans. Ind. Electron.* **2016**, *64*, 5403–5415. [[CrossRef](#)]
15. Mathew, D.; Chinnappa Naidu, R.; Wang, Y.; Busawon, K. Single-stage microinverter with current sensorless control for BIPV system. *IET Renew. Power Gener.* **2021**, *15*, 2468–2479. [[CrossRef](#)]
16. Tsai, C.Y.; Tsai, C.Y. See-through, light-through, and color modules for large-area tandem amorphous/microcrystalline silicon thin-film solar modules: Technology development and practical considerations for building-integrated photovoltaic applications. *Renew. Energy* **2020**, *145*, 2637–2646. [[CrossRef](#)]
17. Derick, M.; Rani, C.; Rajesh, M.; Farrag, M.; Wang, Y.; Busawon, K. An improved optimization technique for estimation of solar photovoltaic parameters. *Sol. Energy* **2017**, *157*, 116–124. [[CrossRef](#)]
18. Mathew, D.; Rani, C.; Kumar, M.R.; Wang, Y.; Binns, R.; Busawon, K. Wind-driven optimization technique for estimation of solar photovoltaic parameters. *IEEE J. Photovolt.* **2017**, *8*, 248–256. [[CrossRef](#)]
19. Esram, T.; Chapman, P.L. Comparison of photovoltaic array maximum power point tracking techniques. *IEEE Trans. Energy Convers.* **2007**, *22*, 439–449. [[CrossRef](#)]
20. Melo, F.C.; Garcia, L.S.; de Freitas, L.C.; Coelho, E.A.; Farias, V.J.; de Freitas, L.C. Proposal of a photovoltaic AC-module with a single-stage transformerless grid-connected boost microinverter. *IEEE Trans. Ind. Electron.* **2017**, *65*, 2289–2301. [[CrossRef](#)]
21. Kumar, A.; Sensarma, P. A four-switch single-stage single-phase buck–boost inverter. *IEEE Trans. Power Electron.* **2016**, *32*, 5282–5292. [[CrossRef](#)]
22. Gautam, V.; Sensarma, P. Design of Ćuk-derived transformerless common-grounded PV microinverter in CCM. *IEEE Trans. Ind. Electron.* **2017**, *64*, 6245–6254. [[CrossRef](#)]
23. Rajeev, M.; Agarwal, V. Analysis and Control of a Novel Transformer-Less Microinverter for PV-Grid Interface. *IEEE J. Photovolt.* **2018**, *8*, 1110–1118. [[CrossRef](#)]
24. Roy, J.; Xia, Y.; Ayyanar, R. High Step-Up Transformerless Inverter for AC Module Applications With Active Power Decoupling. *IEEE Trans. Ind. Electron.* **2018**, *66*, 3891–3901. [[CrossRef](#)]